UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/871,180	05/31/2001	Mark Tetreault	SRT-016	9989

22832 7590 07/06/2005

KIRKPATRICK & LOCKHART NICHOLSON GRAHAM LLP
(FORMERLY KIRKPATRICK & LOCKHART LLP)
75 STATE STREET
BOSTON, MA 02109-1808

EXAMINER	
MASKULINSKI, MICHAEL C	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 07/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/871,180	TETREAULT, MARK	
	Examiner	Art Unit	
	Michael C. Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *14 and 25-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,15-22 and 24* is/are rejected.

7)☒ Claim(s) *10-13 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Office Action

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-9, 19-21, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelley et al., U.S. Patent 6,170,029 B1, and further in view of Nelvin et al., U.S. Patent 6,708,283 B1.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned

by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Referring to claim 1:

a. In column 5, lines 15-34, Kelley et al. teach an apparatus for isolating, in response to a device isolation signal and a bus idle status signal, a device from a bus without interrupting system operation.

b. In column 5, lines 24-26, Kelley et al. disclose that the hot plug controller monitors the bus for an idle bus, to assure that the previous master is off the bus (bus interface logic in communication with the bus, the bus interface logic generating a signal indicating the idle status of the bus)

c. In column 5, line 28, Kelley et al. disclose load control switches (an isolation switch in communication with the bus).

d. In column 5, lines 15-17, Kelley et al. disclose that an operator initiates the hot plug sequence by requesting at a keyboard that a specific adapter be hot plugged (a device isolation control line).

e. In column 5, lines 15-17, Kelley et al. disclose that a hot plug sequence is initiated, however, Kelley et al. don't explicitly disclose a protocol checker logic configured to monitor the validity of bus transactions and to generate a device isolation control signal on a device isolation control line. In column 6, lines 45-63, Nelvin et al. disclose error detection logic that determines a bus controller has failed based on errors in the communications from the bus controller, such as the bus controller using an address with a parity error and in response the hot

plug controller isolates the bus controller. It would have been obvious to one of ordinary skill at the time of the invention to include the protocol violation detector device isolation signal of Nelvin et al. into the system of Kelley et al. A person of ordinary skill in the art would have been motivated to make the modification because it is important to reduce downtime for single points of failure by detecting the failure and having redundant components that are hot-swappable (see Nelvin et al., column 1, lines 46-55).

f. In column 5, lines 26-30, Kelley et al. disclose that the hot plug controller and the load control logic change the state of the set of load control switches at the slot of the hot plug action. That action disconnects the slot and connects the dummy load (isolation control logic in communication with the bus interface logic, the device isolation control line, and the isolation switch)

g. In column 5, lines 24-30, Kelley et al. disclose that the hot plug controller monitors the bus for an idle bus, to assure that the previous master is off the bus. The hot plug controller and the load control logic change the state of the set of load control switches at the slot of the hot plug action. That action disconnects the slot and connects the dummy load (wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus idle status signal from the bus interface logic and the received device isolation signal on the device isolation control line).

Referring to claim 2, in column 5, lines 38-40, Kelley et al. disclose that the hot plug controller (bus interface logic) is capable of changing the states of the load switches, therefore, a state machine is inherent to the hot plug controller of Kelley et al.

Referring to claim 3, although Kelley et al. don't disclose that the hot plug controller (bus interface logic) comprises combinatorial logic for reasons given in column 2, lines 25-33, it is inherent to the system of Kelley et al. because of the need to change states based upon certain signals.

Referring to claim 4, in column 5, lines 24-26, Kelley et al. disclose that the hot plug controller monitors the bus (the bus interface logic monitors all bus transactions).

Referring to claim 5, in column 5, lines 24-29, Kelley et al. disclose that the hot plug controller monitors the bus for an idle bus, to assure that the previous master is off the bus. The hot plug controller and the load control logic change the state of the set of load control switches at the slot of the hot plug action (the bus status signal generated by the bus interface logic indicates that the bus is idle).

Referring to claim 6, although Kelley et al. don't disclose that the isolation control logic comprises combinatorial logic for reasons given in column 2, lines 25-33, it is inherent to the system of Kelley et al. because of the need to change states based upon certain signals.

Referring to claim 7, in column 5, lines 15-17, Kelley et al. disclose that during a hot plug sequence, an operator initiates the sequence by requesting at a keyboard that a specific adapter be hot plugged (the isolation control logic receives the device isolation signal from logic monitoring the operational status of the system).

Referring to claim 8, in column 5, lines 15-21, Kelley et al. disclose that hot plug software along with the device driver quiesces the adapter such that the adapter is not doing operations on the PCI bus. The hot plug controller then isolates the PCI bus via a set of in-line load switches (the isolation control logic receives the device isolation signal from a hot-plug logic element).

Referring to claim 9, in column 3, lines 18-23, Kelley et al. disclose that all four PCI slots have control signal output lines connected to a control signal bus. The control signals applied to the control signal bus include "presence detect" signals from the PCI slots, which indicate presence or absence of a PCI device in each of the four slots (the hot-plug logic element generates the device isolation signal responsive to the physical removal of the device from its slot).

Referring to claims 19 and 24:

a. In column 5, lines 15-17, Kelley et al. disclose that a hot plug sequence is initiated, however, Kelley et al. don't explicitly disclose a protocol checker logic configured to monitor the validity of bus transactions and to generate a device isolation control signal on a device isolation control line. In column 6, lines 45-63, Nelvin et al. disclose error detection logic that determines a bus controller has failed based on errors in the communications from the bus controller, such as the bus controller using an address with a parity error and in response the hot plug controller isolates the bus controller. It would have been obvious to one of ordinary skill at the time of the invention to include the protocol violation detector device isolation signal of Nelvin et al. into the system of Kelley et al. A person of

ordinary skill in the art would have been motivated to make the modification because it is important to reduce downtime for single points of failure by detecting the failure and having redundant components that are hot-swappable (see Nelvin et al., column 1, lines 46-55).

b. In column 5, lines 15-34, Kelley et al. teach a method for isolating a bus device from the bus.

c. In column 5, lines 24-26, Kelley et al. disclose that the hot plug controller monitors the bus for an idle bus, to assure that the previous master is off the bus (receiving a bus idle status signal)

d. In column 5, line 28, Kelley et al. disclose load control switches (an isolation switch in communication with the bus).

e. In column 5, lines 15-17, Kelley et al. disclose that an operator initiates the hot plug sequence by requesting at a keyboard that a specific adapter be hot plugged (a device isolation control line).

f. In column 5, lines 24-30, Kelley et al. disclose that the hot plug controller monitors the bus for an idle bus, to assure that the previous master is off the bus. The hot plug controller and the load control logic change the state of the set of load control switches at the slot of the hot plug action. That action disconnects the slot and connects the dummy load (transmitting an isolation switch control signal responsive to both the received device isolation signal and the received bus idle status signal; and isolating the device from the bus).

Referring to claim 20, in column 5, lines 15-17, Kelley et al. disclose that an operator initiates the hot plug sequence by requesting at a keyboard that a specific adapter be hot plugged (isolating the identified bus device from the bus responsive to the received bus device isolation signal).

Referring to claim 21, in column 4, lines 46-49, Kelley et al. teach inhibiting bus access.

3. Claims 15-18, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kelley et al., U.S. Patent 6,170,029 B1 and Nelvin et al., U.S. Patent 6,708,283 B1, and further in view of Sadana, U.S. Patent 6,453,429 B1.

Referring to claim 15, in column 5, lines 15-17, Kelley et al. disclose that a hot plug sequence is initiated, however, neither Kelley et al. nor Nelvin et al. explicitly disclose that the isolation control logic comprises a timer measuring elapsed time. In column 2, lines 58-61, Sadana discloses that a status circuit is provided for monitoring the first and second units as well as a counting circuit that is measuring periods of bus inactivity during an active bus transfer sequences. It would have been obvious to one of ordinary skill at the time of the invention to include the timer of Sadana into the combined system of Kelley et al. and Nelvin et al. A person of ordinary skill in the art would have been motivated to make the modification because although PCI based components are designed to conform to a standard, there are numerous occasions when the incompatibilities between the different components in the system or bugs in the code, can cause the PCI bus to hang (see Sadana: column 1, lines 44-47).

Therefore, there is a need for a means to detect the bus hang condition in order to prevent system failure. This is provided through the timer of Sadana.

Referring to claim 16, in column 2, lines 58-61, Sadana discloses that a status circuit is provided for monitoring the first and second units as well as a counting circuit that is measuring periods of bus inactivity during an active bus transfer sequences (the timer measures elapsed time relative to a system event).

Referring to claim 17, in column 2, lines 61-64, Sadana discloses a compare circuit that is in processing communication with the first and second units for comparing threshold counts provided with a threshold value circuit (a timeout signal is generated in response to the elapsed time exceeding a predetermined threshold).

Referring to claim 18, in column 8, lines 23-26, Sadana discloses that the id of the master on the bus is trapped (device isolation signal). Further, in column 8, lines 28-32, Sadana discloses that when the bus is hung (a timeout signal is received) the bus is reset after the bus master id is stored (the isolation control logic transmits a bus reset signal responsive to receiving both the device isolation signal and the timeout signal from the timer).

Referring to claim 22, in column 5, lines 15-17, Kelley et al. disclose that a hot plug sequence is initiated, however, Kelley et al. don't explicitly disclose receiving a timeout signal and resetting the bus responsive to receiving both the timeout signal and the bus status idle signal indicating that the bus is not idle. In column 2, lines 58-61, Sadana discloses that a status circuit is provided for monitoring the first and second units as well as a counting circuit that is measuring periods of bus inactivity during an

active bus transfer sequences. Further, in column 8, lines 28-32, Sadana discloses that when the bus is hung (a timeout signal is received and the bus is not idle) the bus is reset. It would have been obvious to one of ordinary skill at the time of the invention to include the timeout signal and bus reset of Sadana into the system of Kelley et al. A person of ordinary skill in the art would have been motivated to make the modification because although PCI based components are designed to conform to a standard, there are numerous occasions when the incompatibilities between the different components in the system or bugs in the code, can cause the PCI bus to hang (see Sadana: column 1, lines 44-47). Therefore, there is a need for a means to detect the bus hang condition in order to prevent system failure. This is provided through the timer of Sadana.

Allowable Subject Matter

3. Claims 10-13 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments with respect to claims 1, 19, and 24 have been considered but are moot in view of the new ground(s) of rejection. The Examiner would like to point out that limitation "protocol checker logic configured to monitor the validity of bus transactions and to generate a device isolation control signal on a device isolation control line" was part of claim 10, which was rejected in the last Office Action. For this reason claims 1, 19, and 24 are currently rejected. If the Applicant intended to put

these claims in condition for allowance, then the Applicant is reminded that claim 13 and all of its limitations and the limitations of the intervening claims must be placed in the independent claims.

5. On page 9, under the section Rejections Under 35 U.S.C. § 102, the Applicant argues, "By contrast, Applicant's claimed invention is automatic and does not require manual user intervention." The Examiner respectfully disagrees. The term automatic does not appear anywhere in the claims nor do the claims hint at it being done automatically.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

SCOTT BADERMAN
PRIMARY EXAMINER